

20V Dual N-Ch Power MOSFET

Feature

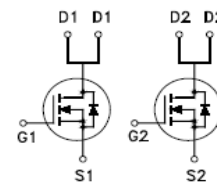
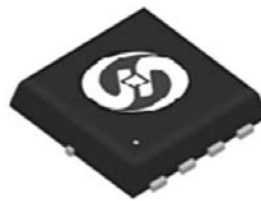
- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

V_{DS}		20	V
$R_{DS(on),typ}$	$V_{GS}=4.5V$	13	mΩ
I_D		7	A

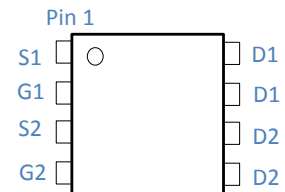
Application

- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial

DFN3x3



Part Number	Package	Marking
HTM150A02	DFN3*3	TM150A02



Absolute Maximum Ratings at $T_J=25^{\circ}C$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current	I_D	$T_C=25^{\circ}C$	7	A
		$T_C=100^{\circ}C$	5	
Drain to Source Voltage	V_{DS}	-	20	V
Gate to Source Voltage	V_{GS}	-	± 12	V
Pulsed Drain Current	I_{DM}	-	28	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.1mH, T_C=25^{\circ}C$	5.0	mJ
Power Dissipation	P_D	$T_C=25^{\circ}C$	2	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	$^{\circ}C$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	62.5	$^{\circ}C/W$
Thermal Resistance Junction-Case	$R_{\theta JC}$	25	$^{\circ}C/W$

Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	0.4	0.8	1.2	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=16V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{GS}=0V, V_{DS}=16V, T_j=125^\circ\text{C}$	-	-	25	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=7A$	-	13	15	$m\Omega$
		$V_{GS}=2.5V, I_D=5A$	-	19	23	
Transconductance	g_{fs}	$V_{DS}=5V, I_D=7A$	-	9	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=10V, f=1\text{MHz}$	-	700	-	pF
Output Capacitance	C_{oss}		-	208	-	
Reverse Transfer Capacitance	C_{riss}		-	187	-	
Total Gate Charge	Q_g	$V_{DD}=10V, I_D=7A, V_{GS}=4.5V$	-	10	-	nC
Gate to Source Charge	Q_{gs}		-	1.8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	3.7	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=1A, V_{GS}=4.5V,$ $R_G=6\Omega,$	-	15	-	ns
Rise time	t_r		-	20	-	
Turn off Delay Time	$t_{d(off)}$		-	30	-	
Fall Time	t_f		-	20	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=2.3A$	-		1.2	V
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Fig 1. Typical Output Characteristics

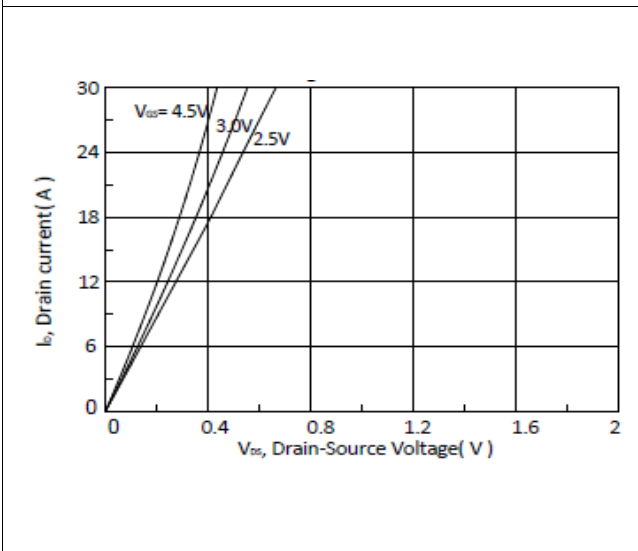


Figure 2. On-Resistance vs. Gate-Source Voltage

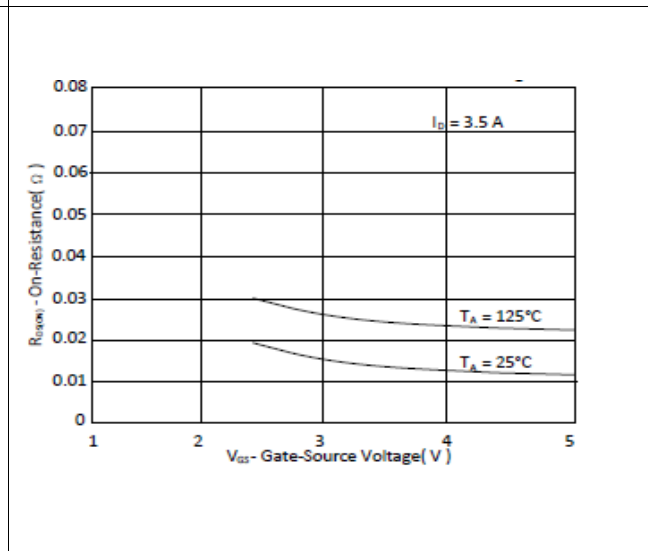


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

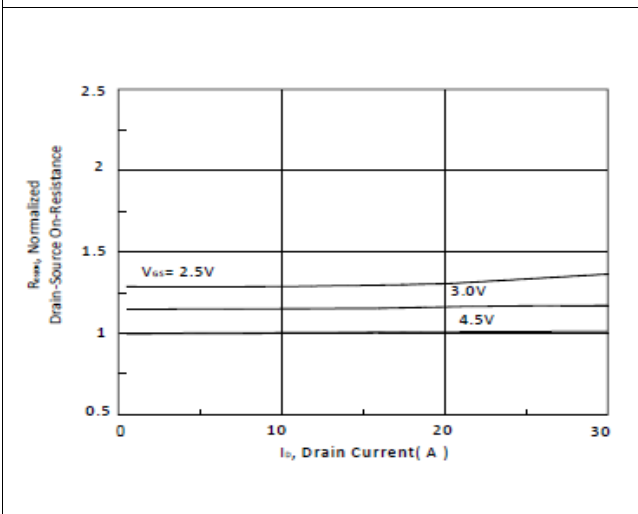


Figure 4. Normalized On-Resistance vs. Junction Temperature

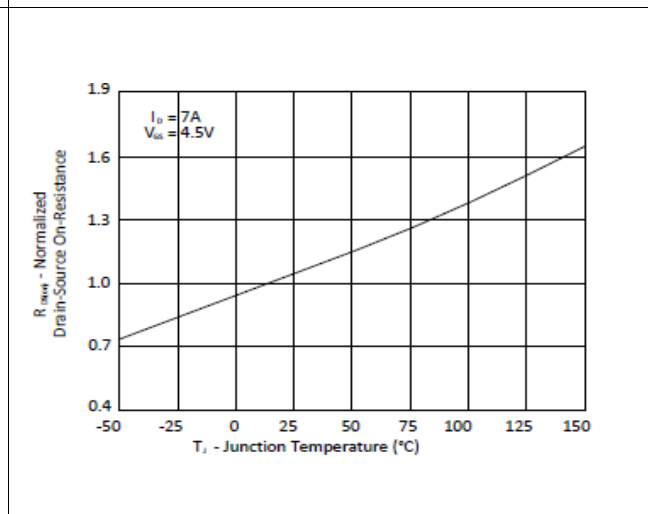


Figure 5. Typical Transfer Characteristics

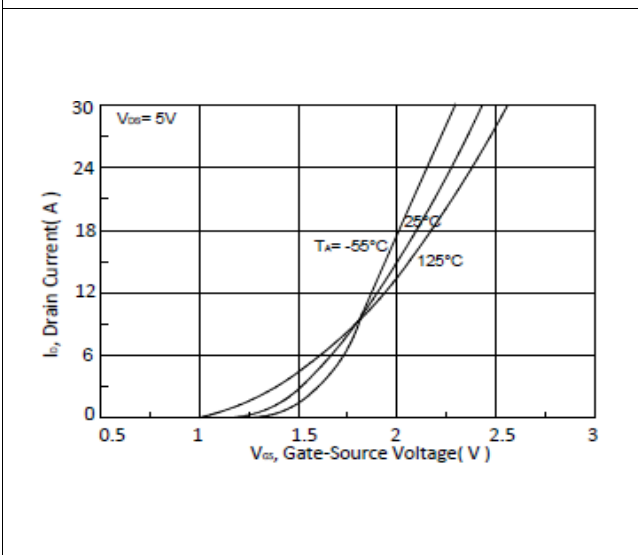


Figure 6. Typical Source-Drain Diode Forward Voltage

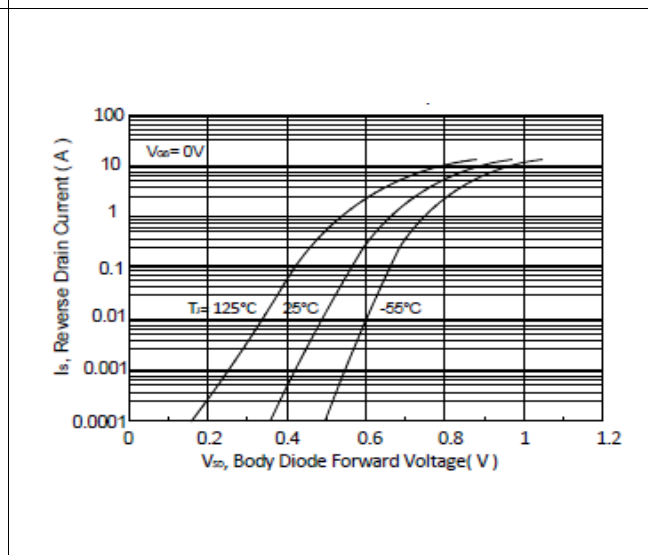


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

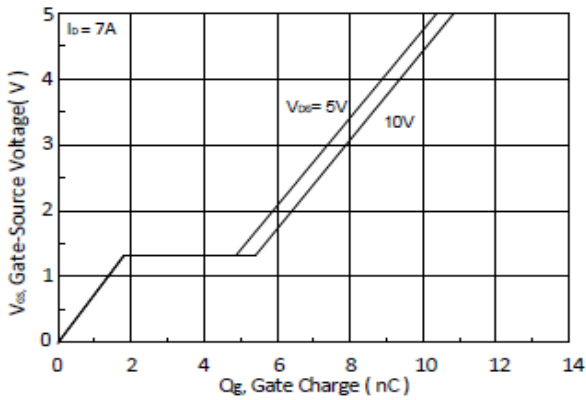


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

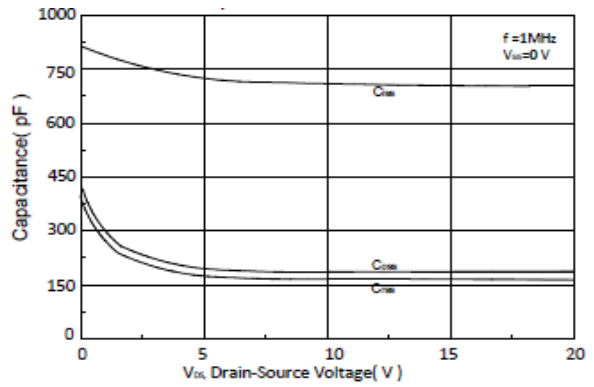


Figure 9. Maximum Safe Operating Area

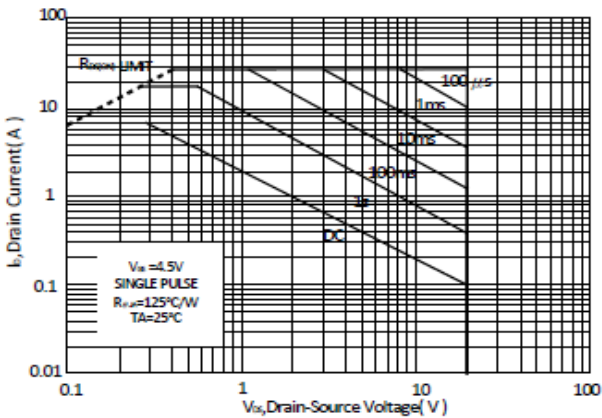


Figure 10. Single Pulse Maximum Power Dissipation

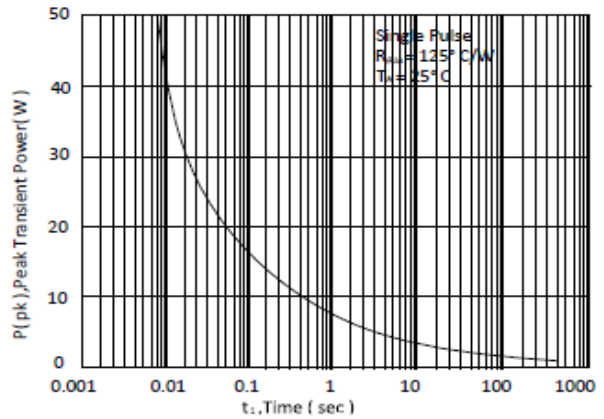
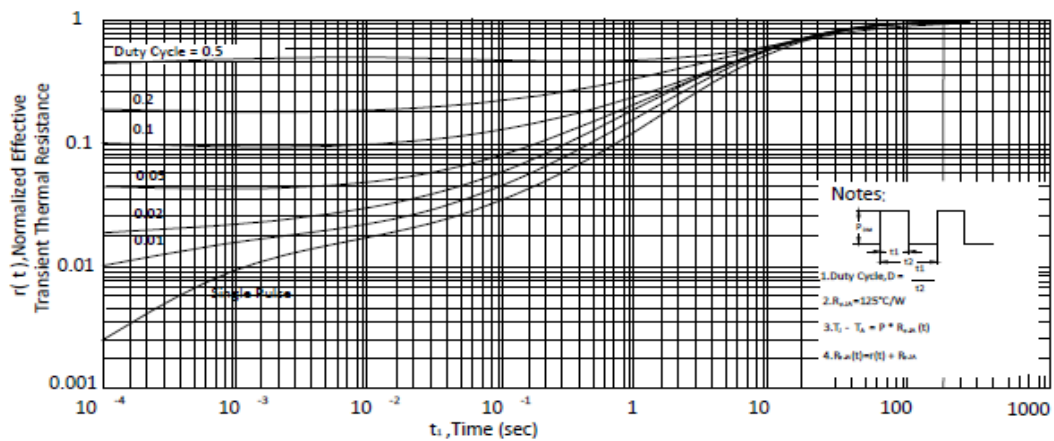
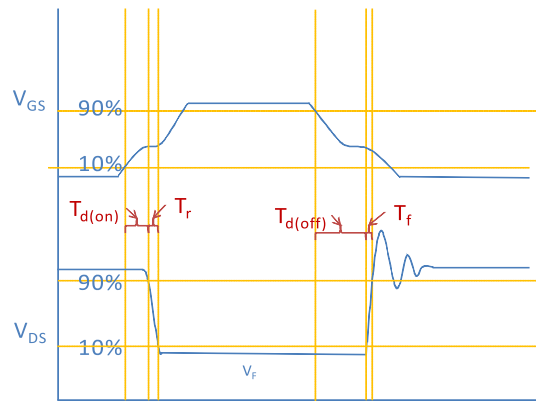
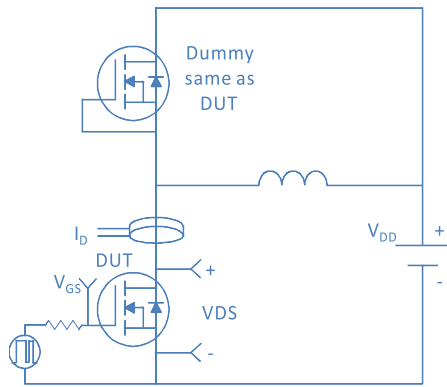


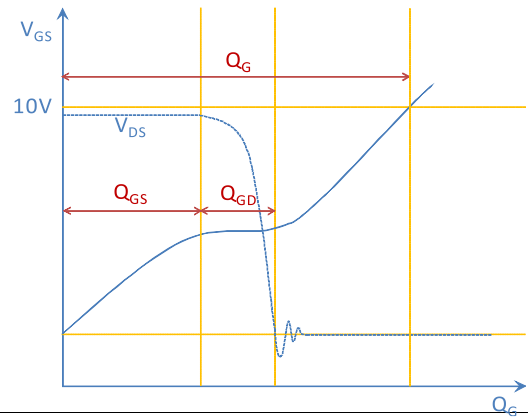
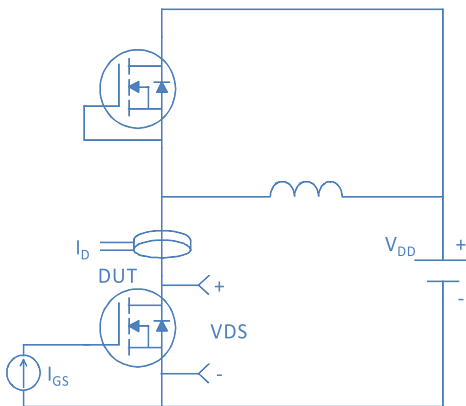
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



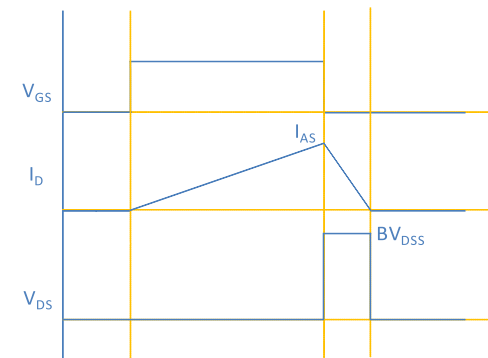
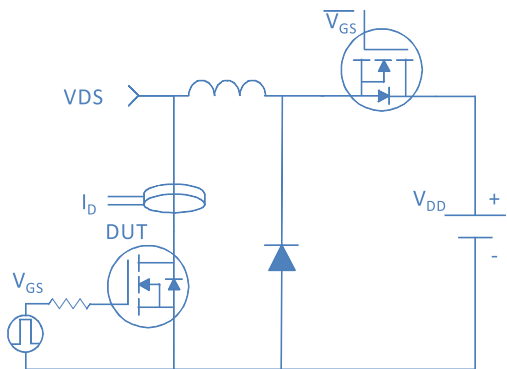
Inductive switching Test



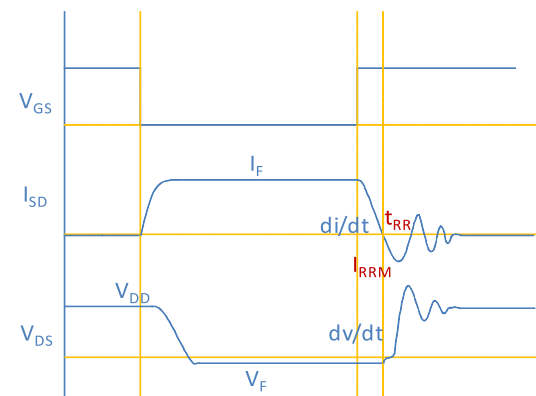
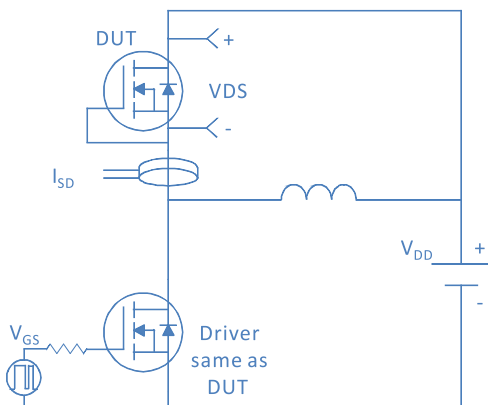
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

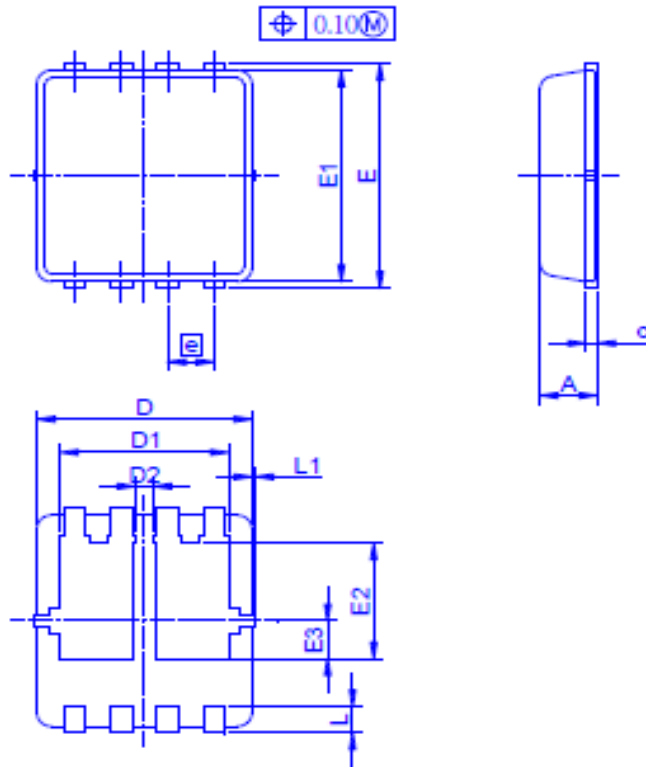


Diode Recovery Test



Package Outline

DFN3x3_P, 8leads



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	$\theta 1$
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°